Description

Integrated circuit with built-in module test

The invention relates to an integrated circuit with built-in module test and especially to an application-specific integrated circuit (ASIC) with a built-in self test (BIST).

Many conventional integrated circuits already have a built-in self test (BIST) by means of which an internal check of the logic functions of the integrated circuit is performed with each new switch-on of the integrated circuit. This makes it possible to test critical chips before any use in the system or, respectively, in a particular hardware environment. Integrated circuits with high complexity such as, for example, INTEL processors already have such a self-test circuit. However, these conventional built-in self-test (BIST) circuits only check the internal logic of an integrated circuit. All output signals going to the outside or input signals present from outside are kept constant and/or not switched through in these circuits.

Although this makes it possible to check the respective integrated circuits in a simple and effective manner, a large proportion of the faults in a module or a board which, for example, result from faulty board connections, contact faults on the circuit board, poor soldering joints, defective I/O connections of the chips etc. remains undetected.

Such faults in a module are usually detected and localized in time-consuming board tests. In these tests, the partially equipped circuit boards are checked for faults but this did not achieve complete testing of the boards.

Another conventional test of a completely configured system consists in that, with each restart, software test routines are initiated which functionally test the module or board. However, this method, too, does not achieve complete testing of the board. Instead, a large proportion of the possible faults on a board remains undetected by this test which leads to failures with extremely high costs only when it is finally used.

The invention is, therefore, based on the object of developing an integrated circuit according to the preamble of claim 1 in such a manner that the costs for testing a module can be considerably reduced.

According to the invention, this object is achieved by means of the features specified in the characterizing clause of claim 1.

According to the invention, the self-test circuit built into the integrated circuit is thus used not only for testing the internal logic but also for testing the external logic located on the module. In this arrangement, in particular, the input/output connections of the integrated circuit are not kept constant but the test pattern generated in the self-test circuit is also output to the chips of the module connected externally via an input/output circuit and a received test response of these

external chips is evaluated with the built-in self-test (BIST) circuit.

The self-test circuit preferably has a test pattern generator for generating a test pattern or, respectively, a signature in the form of pseudo-random vectors and a test response analyzer for evaluating the test response coming from the internal logic and/or external logic. By using test pattern generators and test response analyzers, which are already known, a self-test circuit which tests both the internal logic and the external logic in the module can be implemented with minimum expenditure and with the smallest space requirement in the integrated circuit.

The internal logic and the external logic are preferably tested at the same time, a first section of the test pattern generated by the test pattern generator being output to the internal logic and a second section of the signature being output to the external circuit. Both the internal logic and the external logic provide the respective sections, derived from the signature, of a test response which are compressed and evaluated in the common test response analyzer. The simultaneous testing of the internal and external circuit reduces, in particular, the time expended for the test with each restart of the system. As an alternative, however, a time-sequential test of the internal circuit and the external circuit is also possible which makes it possible to reduce the area required by the self-test circuit in the integrated circuit.

According to a preferred exemplary embodiment, the output circuit exhibits controllable input/output drivers for sending and receiving bidirectional signals, as a result of which the

integrated circuit can also be tested in a hardware environment which, for example, exhibits a bus structure. In particular, use of a control device which controls the drivers of the external components makes it possible to prevent destruction of or damage to the driver stages during the self test.

Furthermore, according to a further preferred exemplary embodiment, the control device of the self-test circuit can be designed in such a manner that two test runs are performed, the first test run being used for initializing undefined chip groups whereas the second test run corresponds to the actual test of the respective components. This makes it possible to also test components with undefined starting levels such as, for example, random-access memories (RAMs) since they are written to in a defined manner in the first test run and are only tested in the second test run.

In the text which follows, the invention will be described in greater detail by means of exemplary embodiments and referring to the drawing, in which:

Figure 1 shows a block diagram of a module according to a first preferred exemplary embodiment, with an integrated circuit and an external circuit;

Figure 2 shows a diagrammatic block diagram of a test pattern generator shown in Figure 1;

Figure 3 shows a diagrammatic block diagram of a test response analyzer shown in Figure 1;

Figure 4 is a representation for illustrating the division of a test pattern into a first part for the internal logic and a second part for the external circuit;

Figure 5 shows a block diagram of a module according to a second preferred exemplary embodiment, with an integrated circuit and an external circuit with bus structure;

Figure 6 is a representation of a bus clock signal of the bus structure shown in Figure 5 for illustrating the chip selection; and

Figure 7 is a block diagram of a random-access memory which can be used, for example, as external component in the bus structure according to Figure 5.

Figure 1 shows a block diagram of a module according to a first preferred exemplary embodiment, comprising an integrated circuit 1, a first external circuit 14 and a second external circuit 15. In the text which follows, the integrated circuit 1 is designated as ASIC 1 since it preferably consists of an application-specific integrated circuit (ASIC). Such integrated circuits are particularly suitable for the present invention since they are specially designed for particular applications in which the hardware or, respectively, the external circuitry is usually specified exactly and is produced in high numbers as system board or module assembly.

The ASIC 1 has an internal logic 2 which consists of a plurality of logic gates and implements the logic function of the ASIC 1. The reference number 3 designates a built-in self-test (BIST) circuit which essentially exhibits a test pattern generator 4 and a test response analyzer 5.

Figure 2 shows a diagrammatic block diagram of the test pattern generator 4. The test pattern generator 4 consists,

for example, of a linear-feedback shift register (LFSR). In this arrangement, a multiplicity of flip-flops 18 are series-connected, the output signal of the last flip-flop being fed back to the input of the first flip-flop. To generate pseudo-random vectors which are used as test pattern 16, they can be located between the respective flip-flop's XOR gates 19 which provide for an exclusive-OR combination of the output signal of a respective flip-flop 18 with the output signal of the last flip-flop. The signal resulting from this exclusive-OR combination is in each case supplied to the input of the following flip-flop. The outputs of the series-connected flip-flops 18 are used as output signal and supply a test pattern or, respectively, a test signature 16 which represents a pseudo-random vector which, with a number of n flip-flops, reproduces 2^n-1 states in an apparently random but repetitive sequence. Such a test pattern or, respectively, such a test signature 16 is eminently suitable for testing highly complex logic circuits since it exhibits an extremely high test severity with the appropriate length of testing.

Figure 3 shows a diagrammatic block diagram of the test response analyzer 5 belonging to the test pattern generator 4 according to figure 2, which is used for compressing and evaluating a test response. The test pattern 16 generated by the test pattern generator 4 is supplied to a circuit to be tested and then generates a test response 17 at its output connections. This test response 17 is supplied to the test response analyzer 5 which, according to figure 3, consists of a multiplicity of series-connected flip-flops 18 and again exhibits a linear-feedback shift register (LFSR). The

test response analyzer 5 is configured in a manner corresponding to the test pattern generator 4 and the circuit to be tested in such a manner that it suitably compresses the test response 17 sent out by the circuit to be tested and outputs an output signal corresponding to the tested logic functions of the circuit to be tested. On the basis of these output signals and with knowledge of the output signals to be expected, it is possible to achieve a sufficiently high test accuracy or severity for detecting errors in the circuit to be tested if the number of test patterns 16 is sufficiently large. The examples for the test pattern generator 4 and the test response analyzer 5 shown in figures 2 and 3 are only used for explaining the principle of generating suitable test patterns and evaluating corresponding test responses. Naturally, the test patterns and test responses, respectively, described above can also be generated and evaluated, respectively, in a different manner.

The special feature of the present invention lies in that a test pattern 16 generated by the test pattern generator 4 is output not only to the internal logic of the ASIC 1 but additionally to the output connections of the integrated circuit or ASIC 1 via an output circuit 7. In contrast to a conventional integrated circuit with built-in self test, in which the output and input connections of the chip are kept constant, at least a part of the test pattern 16 generated by the test pattern generator 4 is present at the output connections of the integrated circuit 1 via output drivers 9 in the integrated circuit 1 according to the invention.

Figure 4 shows a representation for illustrating the division of the test pattern 16 into a first and second part for testing the internal logic 2 and the external logic 14. According to figure 4, the internal logic 2 of the ASIC 1 only consists of one AND gate 20. The external circuit 14 is constructed, for example, of an OR gate 21 and a flip-flop 22. This highly simplified representation of a module to be tested is intended to represent the operation of the ASIC according to the invention in the text which follows. Three test patterns (11, 01, 10) are needed for testing the logic function of the AND gate 20 in the internal logic 2 of the ASIC 1. The logic function of the AND gate 20 can be completely tested with such a test pattern. The OR gate 21 in the external circuit can be tested by three test patterns (01, 10, 00). It is sufficient to check the change in logic level at the output of the flip-flop 22 as a function of the clock signal for a minimum test of the flip-flop 22.

This results in the test pattern sequence (011, 001, 010, 1XX) shown in figure 4, by means of which a minimum test of the internal logic 2 and of the external circuit 14 can be performed. According to the invention, the test pattern generator 4 generates a corresponding test pattern, a first part TM1 of the test pattern 16 being supplied to the internal logic 2 or, respectively, the AND gate 20 whilst a second part TM2 of the test pattern 16 is supplied to the external circuit 14 or, respectively, the OR gate 21 via an output driver 9 and the output connection of the ASIC 1. The reference symbol TA1 here represents the test response of the internal logic 2 whilst TA2 is the test response of the external circuit 14 and is supplied to the test response analyzer 5 via an input driver 9'. The test response TA1 (1, 0, 0, X) output

by the internal logic 2 and the test response TA2 (1, 0, 0, 1) output by the external circuit 14 provide the complete test response 17 (11, 00, 00, X1) which is supplied to the test response analyzer 5 for evaluation. The signals analyzed by the test response analyzer 5 are compared with a signal sequence to be expected, and the test is successful or, respectively, there are no faults in the internal logic 2 and the external logic 14 if expected and received signal sequence match.

If the external circuit 14 consists of a purely combinatorial circuit, clock synchronism and/or defined resetting of the external components is not required. If, however, the external circuit 14 also consists of a sequential chip, i.e. clocked flip-flop 22 or the like, as shown in figure 4, all units included in the self test must operate in a clocked manner and be reset in a defined manner. In this arrangement, the ASIC 1 must have a connection which allows such defined resetting and clocked operation.

Figure 4 shows the ASIC 1 in conjunction with external, purely combinatorial and resettable sequential components which are connected to the ASIC 1 via unidirectional input/output signals 10/11. According to figure 1, an external circuit 15 which has combinatorial and/or sequential components can also communicate with the ASIC 1 via bidirectional signals 12. In this case, the input/output circuit 7 must have controllable input/output drivers 8 which enables the outgoing test patterns and incoming test responses to be separated in time. Such a control is implemented by a control device 6 which preferably controls

the input/output drivers 8 in the input/output circuit 7 in dependence on a clock signal of the bidirectional signals 12. In addition, the control device 6 must switch a driver enable signal via a driver stage 8' to an output connection of the ASIC 1 so that the driver enable signal 13 enables the driver of the external component at the correct time. With the exception of the transmission of the signature and the reception of the test response on one signal line being divided in time, the self test is performed in the same manner as described above.

In the self-test circuit 3 described above, it was assumed that the test pattern 16 generated by the test pattern generator 4 is divided and delivered to the internal logic and the external logic. In the same manner, however, it is also possible to divide the test pattern 16 generated by the test pattern generator 4 in time, the test pattern being transmitted completely to the internal logic 2 in a first time interval whereas it is delivered completely to the external circuit 14 or, respectively, 15 in a second time interval. Similarly, a self-test circuit is conceivable which consists of two test pattern generators and two test response analyzers which are in each case allocated to the internal and external logic. However, the operation corresponds to the operation described above.

Figure 5 shows a block diagram of a module according to a second preferred exemplary embodiment, where the ASIC 1 is connected to a bus structure 12' of the module or, respectively, board. At least one component connected to the bus structure 12' represents a component, the internal states of which cannot be brought to defined values by a reset signal. Such components

are, for example, random-access memories (RAMs) and the like.

Figure 7 shows a block diagram of a random-access memory 23 with its data inputs Din, address inputs ADR, its write enable input WE, its chip enable input CE and its data outputs Dout as can be used, for example, in the circuit according to figure 5.

Such storage chips, the internal states of which cannot be brought to a defined level by a reset signal, require separate treatment during the self test. According to the invention, the control device 6' of the ASIC 1 generates a separate test run before the actual self test until all states used in the external circuit and/or internal logic 2 are initialized. The actual self test is only performed after this initialization in which, for example, data are written into the RAM 23 in a defined manner. The test pattern 16 generated by the test pattern generator 5 can be used for the addressing and writing of the data for this initialization. However, it is also possible to use an initialization circuit which is independent of this and by means of which the respective components 23 are initialized before the actual self test.

A further problem of the bus structure shown in figure 5 is a driver conflict occurring between the components 23. With the currently used CMOS drivers of the chips, such a driver conflict must be avoided in order to prevent damage. However, since a pseudo-random stimulation is normally applied to all

signals and test patterns in the self test according to the invention, a bus conflict must be expected with such random actuation of a respective driver enable signal. To prevent this problem, a chip must drive its output only every 2 x nth clock pulse with n chips connected to a bus structure 12'.

Figure 6 shows a timing diagram of a bus clock signal for illustrating the conflict-free selection of a multiplicity of chips in a bus structure. In the case of the external circuit with two external chips 23 shown in figure 5, the ASIC 1 only drives with clock pulses 0, 6, 12, ... Chip ① only drives its output in clock pulses 2, 8, 14, ... whereas chip ② only drives its output in clock pulses 4, 10, 16, ... All odd clock pulses remain free in order to avoid bus conflicts between the disconnecting driver and the beginning driver. For this method, the driver control signal 13' must be accessible for enabling the respective chip 23 of the external logic. This means that the ASIC 1 may have to exhibit additional output connections in order to supply the driver enable signal 13' to the external circuit under control of the control device 6'.

A further problem may arise in the case where a module has a number of ASICs or integrated circuits 1, respectively, according to the invention. In this case, a number of integrated circuits would attempt to perform a self test of the external circuit. However, this would lead either to falsified test results or even cause damage to the driver stages in the respective components. To solve this problem, the input/output circuit can therefore be selectively deactivated

which prevents the performance of an external test. This means that the test patterns are not sent to the external circuit via the input/output drivers 8 and 9, respectively, and the output connections of the chip as a result of which the chip behaves like a conventional integrated circuit with built-in self test.

The present invention has been described, in particular, by means of an application-specific integrated circuit 1 (ASIC) since such a circuit is particularly tailored to the respective requirements of a closely delimited application. Knowing this application or, respectively, the module in which the ASIC 1 is to be used, it is thus possible also to implement a self test for the external circuit in a simple manner as a result of which a self test is performed with each restart of a module or of a hardware module and a complete board is tested in an extremely simple and inexpensive manner.